AMIGA CHIP SET STRATEGY

Introduction

The objective of the strategy is to refocus effort on the development of a family of high integration custom chips that can be used to build low end to mid range Amiga systems with enhanced features and lower systems costs. The target systems are the A200, A300, A500, A600 and A1000+ class systems. The chip set architecture will also address the possible entry into the game console market.

Mid Range Systems Chip Set Strategy

The present costs of the new Architecture AAA chip set preclude it's use in this class of systems. It's development will continue with it's initial introduction at the high end of the A1000+ and A3000+ 32 bit systems family in 1994. As costs drop over time the AAA chip set is expected to take over all of the 32 bit systems family implementations. This would include the entire Slim Line and desktop family, (A1000+ and A3000+ class systems) in 1995, 1996 time frame.

At present the mid range systems, (32 bit Slim line and desktop systems), will use the AA chip set, Alice and Lisa with the existing Paula. AA's video (256 of 16.6 M colors at VGA resolutions), capabilities are assumed to be adequate for the mid range 32 bit systems with AAA addressing the high end and eventually taking over the entire product family. AA chip set still does not address basic problems in the area of serial port performance and floppy disk drive performance, IDE support and extensive system glue requirements. These problems are addressed by a new super I/O chip that is usable across the entire family of systems, both 16 and 32 bit designs. Also planned is the integration of Paula and Alice into a single chip that is usable across the entire family of 16 and 32 bit systems.

32 BIT MID RANGE SYSTEMS CHIP STRATEGY

1992	**1994**	**1995,96**
AA design chips	**AA plus new chips**	**AAA design**
ALICE	ALICE + PAULA	MONICA
DENISE	DENISE	ANDREA
PAULA	SUPER I/O	LINDA
CIA	"BUSTER"	MARY
CIA	"RAMSEY"	"BUSTER"
"GRAY"		" RAMSEY"
"BUSTER"		
"RAMSEY		

* ALL SYSTEMS WILL USE AN EXTERNAL DAC & KEYBOARD CONTROLLER

Low End Systems Chip Set Strategy

At the low end the basic strategy is to get near AA level of video performance, fix the basic problems with the serial and Floppy drive interfaces, provide a 2 to 4 X performance improvement, reduce the chip count dramatically and reduce systems cost. The strategy is to keep the enhancements to the MINIMUM required, ie no architecture changes or enhancements and no creeping elegance! Reducing the design risks and maintaining 100% software compatibility are of upmost importance.

For the low end systems (16 bit A200, A300, A600) three new chips are proposed.

1) Super I/O - This chip combines the present A300 functions of the two CIAs, Gayle, an enhanced serial port and an enhanced floppy disk drive. This would be packaged in a 160 pin PQFP. This device would be used on both 16 and 32 bit systems. This device could also be provide in two additional versions:

a) A game system version where the serial, parallel, IDE & floppy functions are removed and replaced by the keyboard scan controller

b) A version could also be generated which includes the 68000 core

2) Combination of Alice , Paula and system glue functions into a single 128 pin PQFP. This chip would contain NO functional enhancements to either Alice or Paula and would be used in both 16 and 32 bit systems designs.

3) A new LOW COST Lisa. The chip would be designed to support both a 16 and 32 bit chip RAM with a 2x bandwidth increase over ECS in 16 bit mode and a 4X increase in 32 bit mode. The cost reduction is achieved by deceasing the existing Lisa pallet size from 256 of 16.6 million colors to 256 of 32K colors. The sprite size could also be reduced from 64 bits to 32 bits.

LOW END SYSTEMS CHIP STRATEGY

1991	1993, 1994	1994,95
ECS BASED DESIGNS	**NEW AA - DESIGNS**	**NEW AA - & 68K CORE**
AGNUS	ALICE + PAULA	ALICE +PAULA
DENISE	NEW LC LISA	NEW LC LISA + DAC
PAULA	SUPER I/O	SUPER I/O + 68K +KBMPU
CIA		
CIA		
GAYLE		
DAC 3x4	DAC 3x5	
KBD CNTRL	VENDOR MPU KBD CNTRL	

Chip Development Summary

In summary to support both the low end and mid range systems requirements three new chip developments are required:

1) Super I/O (could possibly be a standard cell using industry macros for the enhanced serial and floppy drive features)

2) Combined Alice and Paula

3) Low Cost Lisa

The strategy requires retaining and supporting the following AA chips

1) Alice until the Alice + Paula combination exists

2) Paula until the Alice + Paula combination exists

3) Existing Lisa

The strategy further assumes the continued development of the AAA chip set for mid range systems and the development of gate arrays to support the "BUSTER" and "RAMSEY" functions.

Super I/O Chip Description

Figure 1.0 is a block diagram and pin out for the super I/O chip. This chip is defined for use in both low end 16 bit and mid range 32 bit systems. It combines the functions of Gary, Gayle, the Two CIAs and provides enhanced serial and Floppy drive support. It would attach to the 68000's local bus (as CIAs to today) with out additional glue. Combining the CIA functions with either Alice or Lisa would require that they be placed on the chip RAM bus and increasing the opportunity for lock out during high resolution & color modes. The enhanced serial and Floppy drive functions are implemented using industry standard UARTS and FDD controllers which are mux with the existing Paula implementations. The Mux allows software control of the existing or new serial and floppy drive ports selection permitting an exact compatibility mode. Since Paula implements only the serial interfaces for the Serial port and the FDD port, a very few interface lines are required to support the mux function.

The following is a brief summary of the functions in the Super I/O chip:

- Gary or Gayle clock generation
- Gary or Gayle FDD interface circuits
- Gary or Gayle Chip Select Decodes

- ROM chip select
- Gayle IDE Hard Disk control signal generation
- Gayle PCMCIA support
    - control for buffered & non Buffered PCMCIA
    - Flash & EPROM programming control
    - enhancement for DMA support
- New FDD controller and mux (use industry standard macro)
- New Serial port controller and mux (use industry standard macro)
- Odd CIA port functions
- Even CIA port functions
- DMA support for FDD & PCMCIA
- Basic Fast RAM control Signals
- 68K bus interface
- misc signal and glue removal support

The proposed partitioning requires 140 signals, thus a 160 pin package is proposed.

Similar Combos are used in the PCs. A two serial, FDD, IDE, Parallel port & Keyboard controller (8042 MPU) , RTC & CMOS memory PC combo cost in the $7 range today in a 160 pin PQFP package.

ALICE & PAULA Combo Chip Description

Since Alice and Paula both reside on the Chip RAM data bus and are controlled by the Register Address bus combining them results in a modest increase in total Pin count. The two chips share a total of 25 signals:

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- D0-D15
- RA 1-8
- DMAL

Combining the 84 pin Alice with the 48 pin Paula a 132 pin package. However if the 25 common signals are removed the signal, power and ground requirement is 115. A package size of 128 pin appears possible assuming some glue reduction pins are used.

With Alice's device count at 39500 and Paula's at 21857, the combo chip would be approximately 61,357 transistors. ~ 100K Tn CMOS.

Cost Reduced Lisa Chip Description

This chip would be derived directly from the existing AA Lisa. The objective would be to support two modes of operation, a 16 bit and a 32 bit. In the 16 bit mode a 2X bandwidth increase over the ECS would be achieved using page mode accesses. This would allow 256 color support in interlaced NTSC/PAL

screens and 16 colors in VGA non interlaced screen modes. When additional chip RAM is added, it is added in a parallel mode expanding chip RAM to 32 bits. This allows a 4X bandwidth increase over the ECS. (AA bandwidth and resolution). In this mode VGA non interlaced screens could support 256 colors.

Reduction in cost is primarily achieved by reducing the pallet size from the 25 bit pallet (16.6 million colors) to a 16 bit (32K color) Pallet. It is also assumed that the 64 pixel wide sprites can be reduced to 32 pixels wide. The existing Lisa contains 124,500 transistors. If 50% of the die is in the pallet then 62,250 devices can be reduced by the ratio of the pallet size reduction or:

Reduction = 62,250 x 16/25 = 39,840 transistors

L C Alice device count = 124.500 - 39,840 = 84,660 Transistors

It is assumed that the package size (84 pin) would not have to change.

Summary of New Chips

chip	package size	devices or gates	estimated cost
LC Lisa	84 pin	84,660 devices	
Alice + Paula	128 pin	61,357 devices	
super I/O	160 pin	13,000 gates	

Note: combining a LC Lisa and Alice & Paula combo results in a device count of 146,017 transistors and would easily fit in a 208 PQFP package. From a total device count perspective this chip has approximately the same devices a the AAA Monica chip! The ultimate low end system would be this Super Amiga chip and the super I/O device with an integrated 68K core.

Low End Systems Glue Absorption

In the present A300 implementation a significant number of glue TTL parts are still required. The following is a summary of these parts and how they would be effected by the new chip set.

chip	use	status	cost
74F258	ext clk sel / inv	removed	should be ASIC anyways.
74F139	CAS for exp RAM	removed	
74F00	BCAS timing	removed	
2X 74LS245	68K Bus ISO	remain	
74LS74	PAL goodies	removed	
2X 74HTC244	DENISE buffers	removed	CMOS now (free)
74LS245	PCMCIA cntrl buf	removed	
2X 74LS245	PCMCIA data buf	remain	
74LS157	Aux Port MUX en	removed	
74LS02	PCMCIA control	removed	

15 chips

8 Removed

3X 74LS244	PCMCIA addr buf	remain	
74F02	PCMCIA glue	removed	
totals		14 / 7 removed	

Low End System Implementation Using the New chip Set

Figure 2.0 is a block diagram of a low end system implementation using the proposed new chips and partitioning

Fig 2.0

16.3.1 A300/A600 SYSTEMS (3 CHIP DESIGN)

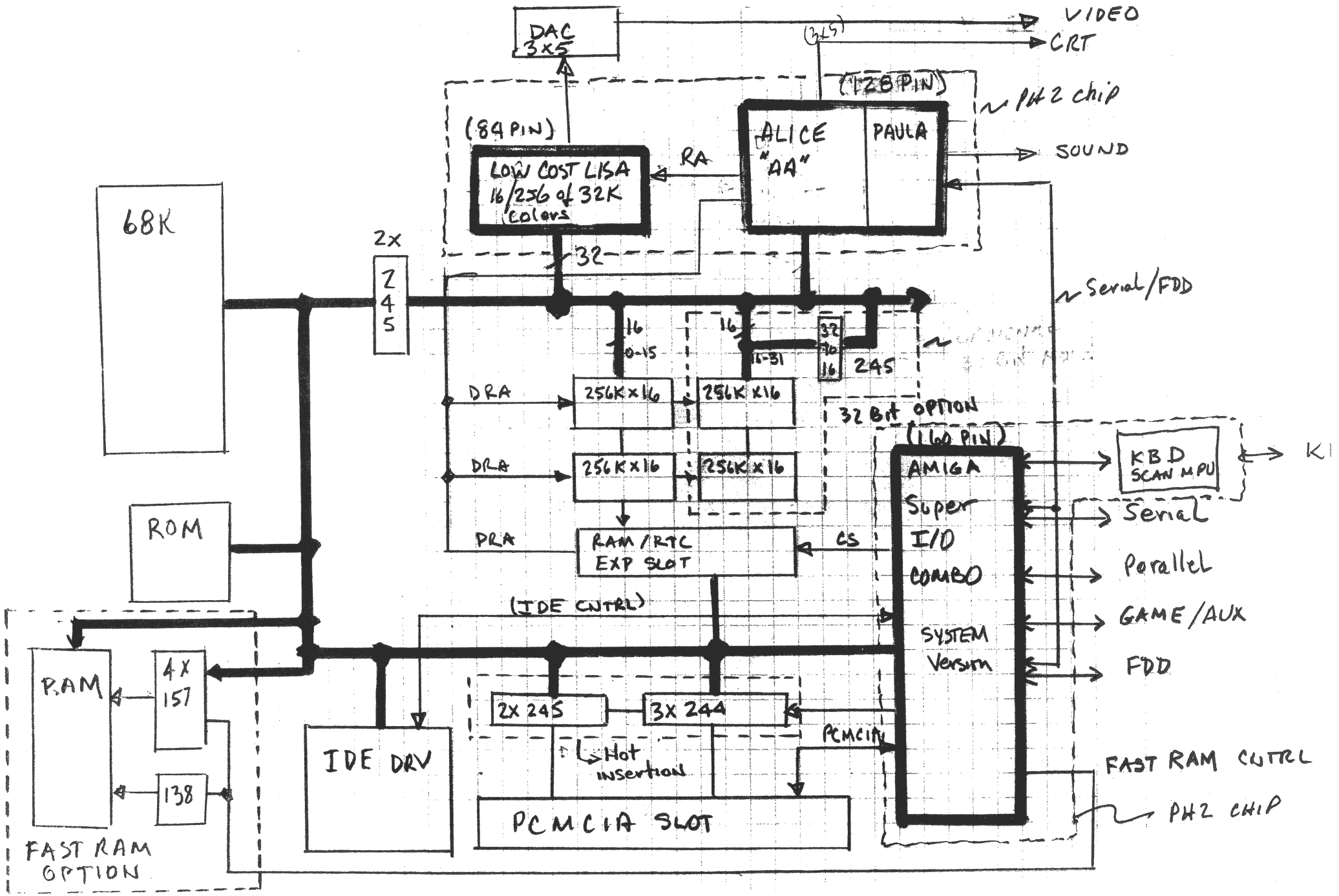
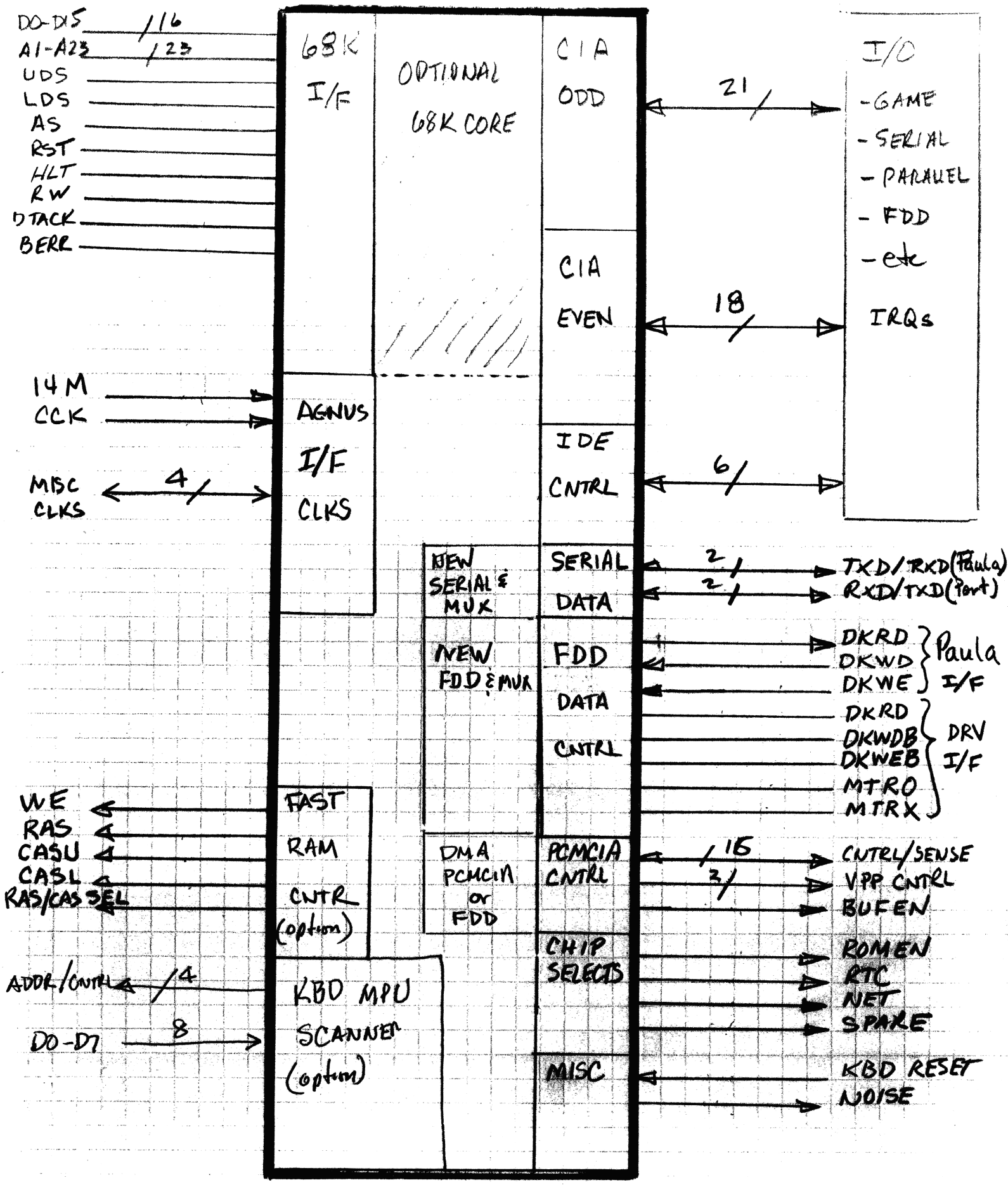


Fig 1.0

NEW AMIGA 3000 Super I/O



LOW END SYSTEMS CHIP STRATEGY